What is claimed is:

1. A circuit for analog-to-digital conversion, comprising:

a calibration reference circuit that is configured to provide a calibration reference signal, wherein the calibration reference circuit is included within an integrated circuit; and

a conversion circuit that is included within the integrated circuit, wherein the conversion circuit includes:

a comparison reference circuit that is configured to provide a plurality of references signals; and

a comparison circuit that is configured to provide a plurality of comparator output signals in response to the plurality of reference signals and a comparison input signal, wherein the comparison input signal is generated from the calibration reference signal if a calibration signal is asserted.

2. The circuit of Claim 1, wherein the calibration reference circuit is arranged such that:

if the calibration signal is asserted, the calibration reference circuit is enabled; and

if the calibration signal is unasserted, the calibration reference circuit is disabled such that the calibration reference circuit consumes substantially no power.

3. The circuit of Claim 1, wherein the calibration reference circuit includes a first resistor ladder, the comparison reference circuit includes a second resistor ladder, and wherein the first resistor ladder is significantly larger than the second resistor ladder.

4. The circuit of Claim 1, wherein the calibration reference circuit includes a resistor ladder, and wherein the resistor ladder is arranged to provide the calibration reference signal such that the calibration reference signal includes one of a plurality of precisely spaced voltages that is selected in response to a calibration reference control signal.

5. The circuit of Claim 1, wherein the comparison circuit includes:

an amplifier circuit comprising a plurality of amplifiers, wherein the amplifier circuit is configured to provide a plurality of amplifier output signals in response to the plurality of reference signals and the comparison input signal; and

a comparator circuit comprising a plurality of comparators, wherein the comparator circuit is configured to provide the plurality of comparator output signals in response to the plurality of amplifier output signals.

6. The circuit of Claim 5, further comprising:

a calibration control circuit, wherein the calibration control circuit is a digital circuit that is arranged to provide an adjustment signal in response to a quantity X of the plurality of comparator output signals,

wherein the amplifier circuit includes a first amplifier array including Y differential pairs and the amplifier circuit further includes a second amplifier array including Z differential pairs, the second amplifier array is folded according to an order of folding F, Y/Z is a multiple of F, and wherein X=Y/(F*Z).

7. The circuit of Claim 5, further comprising:

a calibration control circuit, wherein the calibration control circuit is a digital circuit that is arranged to receive at least one of the plurality of comparator output signals provide an adjustment signal in response to the at least one of the plurality of comparator output signals, and wherein the comparison control circuit further includes:

a coarse reference circuit that is arranged to provide a plurality of coarse reference voltages;

a coarse reference circuit that is arranged to provide a coarse channel output signal from the plurality of coarse reference voltages and the comparison input signal; and

a decoder circuit that is arranged to provide a digital output signal from the coarse channel output signal and the plurality of comparator output voltages.

8. The circuit of Claim 5, further comprising:

a calibration control circuit, wherein the calibration control circuit is a digital circuit that is arranged to receive one of the plurality of comparator output signals, the amplifier circuit includes a plurality of input stages, and wherein the calibration control circuit is arranged to, for each of the input stages in the amplifier circuit, calibrate a zero-crossing that is associated with the input stage in response to the one of the plurality of comparator output signals.

9. The circuit of Claim 1, further comprising:

a multiplexer circuit that is included within the integrated circuit, wherein the multiplexer circuit is configured to provide a multiplexer output signal that corresponds to:

if a calibration signal is asserted, the calibration reference signal; and

if the calibration signal is unasserted, an analog input signal,

wherein the first comparison input signal is generated from the multiplexer output signal.

10. The circuit of Claim 9, further comprising:

a sample-and-hold circuit that is configured to generate the comparison input signal from the multiplexer output signal.

11. The circuit of Claim 1, further comprising:

a calibration circuit that is configured to provide an adjustment signal in response to a feedback signal that includes at least one of the plurality of comparator output signals,

wherein the comparison circuit is arranged to receive the adjustment signal, and wherein the comparison circuit is further arranged such that an offset voltage is adjusted in response to the adjustment signal.

12. The circuit of Claim 11, wherein the adjustment signal includes an adjustment current, the conversion circuit includes a resistor circuit, the conversion circuit is arranged such that the adjustment current is provided to the resistor, and wherein the

calibration circuit is configured to provide the adjustment current such that the adjustment current is substantially inversely proportional to a resistance that is associated with the resistor circuit.

13. The circuit of Claim 11, wherein the calibration control signal is asserted during a calibration phase and during a pre-calibration phase, the calibration circuit is configured to provide the control signal during the calibration phase, the calibration circuit is further configured to provide another adjustment signal in response to the feedback signal during a pre-calibration phase, the comparison reference circuit includes a resistor ladder that is configured to provide the plurality of reference signals in response to a current, and wherein the resistor ladder is arranged such that the current is adjustable responsive to the other control signal.

14. The circuit of Claim 1, further comprising:

another conversion circuit that is included within the integrated circuit, wherein the other conversion circuit includes:

another comparison reference circuit that is configured to provide another plurality of references signals; and

another comparison circuit that is configured to provide another plurality of comparator output signals in response to the other plurality of reference signals and another comparison input signal, wherein the other comparison input signal is generated from the calibration reference signal if the calibration signal is asserted

15. The circuit of Claim 14, further comprising:

a calibration circuit that is configured to provide an adjustment signal in response to a feedback signal that includes at least one of the plurality of comparator output signals, and further configured to provide another adjustment signal in response to another feedback signal that includes at least one of the other plurality of comparator output signals,

wherein the comparison circuit is arranged to receive the adjustment signal and to adjust an offset voltage in response to the adjustment signal, and wherein the other

comparison circuit is arranged to receive the other adjustment signal, and to adjust another offset voltage in response to the other adjustment signal.

16. The circuit of Claim 1, wherein the calibration reference circuit is arranged to generate a plurality of calibration reference voltages, and further arranged such that one of the plurality of calibration reference voltages is selected as the calibration reference signal in response to a calibration control signal.

17. The circuit of Claim 16, wherein the calibration reference circuit includes a resistor ladder, and wherein the calibration reference circuit is further arranged such that Kelvin tapping is employed to provide the plurality of calibration references from the resistor ladder.

18. The circuit of Claim 16, further comprising:

a calibration control circuit that is configured to provide the calibration control signal such that, during a first time interval, the calibration control signal provides each of the plurality of calibration reference voltages in turn, and further configured to provide an adjustment signal in response to a feedback signal that includes at least one of the plurality of comparator output signals, wherein the comparison circuit is arranged to receive the adjustment signal, and the comparison circuit is further arranged to adjust an offset voltage in response to the adjustment signal.

19. The circuit of Claim 18, wherein the calibration control signal is configured to repeatedly provide each of the plurality of calibration reference voltages in turn during a later time interval, wherein the adjustment signal has an associated value, and wherein the calibration control circuit is further configured to provide the adjustment signal such that:

if the feedback signal is associated with a first logical level, the associated value is increased by an adjustment amount, wherein the adjustment amount is relatively large during the first time interval, and wherein the adjustment amount is relatively small during the later time interval; and

if the feedback signal is associated with a second logic level, the associated value is decreased by the adjustment amount.

20. A circuit for analog-to-digital conversion, comprising:

a calibration reference circuit that is configured to provide a calibration reference voltage; and

an interleaved conversion circuit that is interleaved such that the conversion circuit includes a plurality of conversion circuits, wherein each of the plurality of conversion circuits includes:

a comparison reference circuit that is configured to provide a plurality of reference signals; and

a comparison circuit that is configured to provide a plurality of comparator output signals in response to a comparison input signal and the plurality of reference signals, wherein each of the comparison inputs signals is generated from the calibration reference signal if a calibration signal is asserted.

21. The circuit of Claim 20, further comprising:

a calibration circuit that is configured to provide a calibration control signal and a plurality of adjustment signals, wherein the calibration reference circuit is arranged to generate a plurality of calibration reference voltages, and the calibration reference circuit is further arranged such that one of the plurality of calibration reference voltages is selected as the calibration reference signal in response to a calibration control signal, each of the plurality of comparison circuits is configured to provide a feedback signal that includes at least one of the plurality of comparator output signals that is associated with the comparison circuit, each of the plurality of comparison circuits is arranged to receive a corresponding one of the plurality of adjustment signals, each of the comparison circuits is arranged such that an offset voltage that is associated with the comparison circuit is adjusted in response to the corresponding adjustment signal, and wherein the calibration circuit is configured to provide the plurality of adjustment signals such that each of the plurality of adjustment signals is provided in response to a corresponding one of the feedback signals.

22. A circuit for analog-to-digital conversion, comprising:

a means for providing a calibration reference signal, wherein the means for providing the calibration reference signal is included within an integrated circuit; and

a means for conversion that is included within the integrated circuit, wherein the means for conversion includes:

a means for providing a plurality of references signals; and

a means for providing a plurality of comparator output signals in response to the plurality of reference signals and a comparison input signal, wherein the comparison input signal is generated from the calibration reference signal if a calibration signal is asserted.